SSU and SSD Commissioning Status

Commissioning took place between June 28th and July 5th. The primary goal was to bring up both SSU and SSD circuits to its nominal (during STEP 4 run) current values following the previously agreed commissioning plan. Most of the steps have been accomplished already between May 25th and May 30th commissioning work.

The following have been completed:

1. Both SSU and SSD dump circuits have been reworked and checked. The expected current decays were observed during a manual quench trip.
2. New software for the EPIC readout has been introduced and successfully tested for both SSU and SSD QC programs.
3. The filter values for both SSU and SSD coil circuits have been changed form 1 to 10 ms values.
4. All QD channels were tested by injected known voltage values and read them out by the QD software. It was also verified that by bypassing the trip values proper action is taken by the QD.
5. All circuits were re-balanced and the threshold values have been set:
    a. LTS sum set to 20 mV
    b. HTS sum set to 2mV
    c. LTS for EDP opening set to 10 MV
    d. HTS for EDP opening set to 1 mV
    e. M1 and M2 circuit balancing utilized the Idot signals for three magnet circuits: Idot(E1-C-E2), Idot(M1) and Idot(M2). The E1-C-E2 circuit utilized Half-Half coil balancing technique: M1 threshold was set to 150 mV. M2 and E1-C-E2 thresholds were set to 100 mV.
6. SSU E-C-E circuit was ramped up to the newly established nominal values successfully but during ramp down the circuit has tripped. During this trip ground fault also occurred.
7. SSD E-C-E circuit was ramped up to the newly established nominal values successfully. The current was hold for 20 minutes and successfully was ramped down to zero A value.
8. SSD and SSU E-C-E circuits have been ramped together to the new nominal values. During the up-ramp over 200 A SSU tripped and the magnet current were discharged through the discharge diode pack. During the ramp down of the SSD E-C-E circuit there was quench event. The Half-Half coil circuit detected a quench event and opened the contactor. There was also about the same time AGFD trip present. About 25 sec after the the trip was detected the LTS tripped as well and forced the current into the inner diode circuit. This caused a quench.
9. All circuits have been checked out and no anomalies have been observed.
10. We have tested the SSU and SSD circuits in short circuit mode for more than 12 hours and no spurious AGFD trips were observed.